NETWORK ROUTER INTEGRATED ONTO A SILICON CHIP

ABSTRACT OF THE DISCLOSURE

A router is integrated onto a single silicon chip and includes an internal bus that couples multiple data receive and transmit channels to a central processing unit. The channels each have an external interface for connecting to different LAN or WAN networks. The serial channels are convertible into one or more time division multiplexed (TDM) channels. A time slot assigner (TSA) assembles and disassembles data packets transferred in TDM formats, such as ISDN. The serial channels are used for separately processing data packets in each TDM time slot. The TSA is programmable to operate with different TDM formats. A single direct memory access controller (DMAC) is coupled to each serial channel and an Ethernet channel and conducts data transfers on the internal router bus through a common port. The DMAC uses a novel bus protocol that provides selectable bandwidth allocation for each channel. The router architecture includes different interface circuitry which is also integrated onto the silicon chip. The interface circuitry includes user definable input/output (I/O) pins with programmable pulse width detection. The user definable I/O provides synchronous and asynchronous interfacing to peripheral devices with different timing constraints. The interface circuitry also includes a DRAM controller having a programmable timing control circuit that operates with memory devices having different timing and memory block sizes.